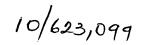
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	M844	2005-10-03	16	Y	2006-04-04 11:37:05.0	MLe _
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<u>#1</u>	((fault-tolerant <in>metadata) <and> (non-fault-tolerant<in>metadata))<and> (redundancy check<in>metadata)</in></and></in></and></in>	0
<u>#2</u>	((fault-tolerant <in>metadata) <and> (non-fault-tolerant<in>metadata))<and> (redundancy<in>metadata)</in></and></in></and></in>	4
<u>#3</u>	((fault-tolerant <in>metadata) <and> (non-fault-tolerant<in>metadata))<and> (redundancy<in>metadata)</in></and></in></and></in>	4
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<u>#6</u>	((fault-tolerant <in>metadata) <and> (non-fault-tolerant<in>metadata))<and> (redundancy<in>metadata)</in></and></in></and></in>	4
<u>#7</u>	((redundant <in>metadata) <and> (non-redundant<in>metadata))<and> (fault-tolerant<in>metadata)</in></and></in></and></in>	9
<u>#8</u>	((redundant <in>metadata) <and> (non-redundant<in>metadata))<and> (fault-tolerant<in>metadata)</in></and></in></and></in>	9
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#11	((redundant <in>metadata) <and> (non-redundant<in>metadata))<and> (fault-tolerant<in>metadata)</in></and></in></and></in>	9
<u>#12</u>	((decode <in>metadata) <and> (non-redundant<in>metadata))<and> (fault-tolerant<in>metadata)</in></and></in></and></in>	0



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Understanding fault-tolerant distributed systems

Flavin Cristian

February 1991 Communications of the ACM, Volume 34 Issue 2

Publisher: ACM Press

Full text available: pdf(6.17 MB)

Additional Information: full citation, references, citings, index terms, review

Reliability Issues in Computing System Design

B. Randell, P. Lee, P. C. Treleaven

June 1978 ACM Computing Surveys (CSUR), Volume 10 Issue 2

Publisher: ACM Press

Full text available: pdf(3.95 MB)

Additional Information: full citation, references, citings, index terms

Emerging areas: Fault-tolerant platforms for automotive safety-critical applications

M. Baleani, A. Ferrari, L. Mangeruca, A. Sangiovanni-Vincentelli, Maurizio Peri, Saverio Pezzini

October 2003 Proceedings of the 2003 international conference on Compilers, architecture and synthesis embedded systems

Publisher: ACM Press

Full text available: pdf(736.40 KB)

Additional Information: full citation, abstract, references, citings, index terms

Fault-tolerant electronic sub-systems are becoming a standard requirement in the automotive industrial sector as electronics becomes pervasive in present cars. We address the issue of fault tolerant chip architectures for autom applications. We begin by reviewing fault-tolerant architectures commonly used in other industrial domains where tolerant electronics has been a must for a number of years, e.g., the aircraft manufacturing industrial sector. We proceed to investigate how t ...

Keywords: VLSI, automotive, fault-tolerant, multi-processor, safety critical, system-on-a-chip

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Steven K. Reinhardt, Shubhendu S. Mukherjee May 2000

ACM SIGARCH Computer Architecture News, Proceedings of the 27th annual international symposium on Computer architecture ISCA '00, Volume 28 Issue 2



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Relevance

181 A novel approach to accurate timing verification using RTL descriptions

K. Roy, J. A. Abraham June 1989

Proceedings of the 26th ACM/IEEE conference on Design automation

Publisher: ACM Press

Full text available: pdf(515.50 KB)

Additional Information: full citation, abstract, references, citings, index terms

Timing verification is a critical part of VLSI circuit design. A new approach to timing verification using Register Tr Level (RTL) descriptions is presented, which eliminates false paths that occur due to (i) redundancy, (ii) reconverfanout or (iii) control signal constraints, and generates a test for the critical paths. High level instructions of the used to test for any timing violations. An algorithm to identify a ...

182 Special session on reconfigurable computing: Designing and testing fault-tolerant techniques for SRAM-ba

FPGAs

Fernanda Lima Kastensmidt, Gustavo Neuberger, Luigi Carro, Ricardo Reis April 2004 Proceedings of the 1st conference on Computing frontiers

Publisher: ACM Press

Full text available: pdf(390.51 KB)

Additional Information: full citation, abstract, references, index terms

This paper discusses fault-tolerant techniques for SRAM-based FPGAs. These techniques can be based on circuit I modifications, with obvious modifications in the programmable architecture, or they can be implemented at the h description, without modification in the FPGA architecture. The high-level method presented in this work is basec Modular Redundancy (TMR) and a combination of Duplication Modular Redundancy (DMR) with Concurrent Error (CED) techniques, which ...

Keywords: FPGA, fault-tolerance

183 Live-structure dataflow analysis for Prolog

Anne Mulkers, William Winsborough, Maurice Bruynooghe

March 1994 ACM Transactions on Programming Languages and Systems (TOPLAS), Volume 16 Issue 2

Publisher: ACM Press

Full text available: pdf(3.59 MB)

Additional Information: full citation, abstract, references, citings, index terms, review

For the class of applicative programming languages, efficient methods for reclaiming the memory occupied by re structures constitute an important aspect of current implementations. The present article addresses the problem reuse for logic programs through program analysis rather than by run-time garbage collection. The aim is to deri time properties that can be used at compile time to specialize the target code for a program according to a given Interferen S, 10/623,099
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L2	269	(714/12).ccls.	US-PGPUB; USPAT	OR	ON	2006/09/21 22:33
L3	522	(714/13).ccls.	US-PGPUB; USPAT	OR	ON	2006/09/21 22:33
L4	16302	fault-toleran\$4 or (fault adj toleran\$4)	US-PGPUB; USPAT	OR	ON	2006/09/21 22:34
L6	19910	fault-toleran\$4 or (fault adj toleran\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/21 22:35
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